THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	
Inventors: Charles HARTMAN et al.	Confirmation No. 9039
U.S. Patent Application No. 10/629,940	Group Art Unit: 2111
Filed: July 29, 2003	Examiner: Christopher Anthony Daley
For: CONFIGURABLE I/O BUS ARCHITECTURE	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attn: BOARD OF PATENT APPEALS AND INTERFERENCES

BRIEF ON APPEAL

This brief is in furtherance of the Notice of Appeal, filed in this case on February 26, 2008.

The fees required under § 1.17(f) and any required petition for extension of time for filing this brief and fees therefore, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

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I. Real Party in Interest

The real party in interest is Hewlett-Packard Development Company, L.P., a Texas limited partnership.

II. Related Appeals and Interferences

There are no other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this appeal.

III. Status of Claims

A. Total Number of Claims in Application

There is a total of 18 claims in the application, which are identified as claims 1-18.

B. Status of all the Claims

Claims 1-18 are pending.

Claims 1-18 are rejected.

C. Claims on Appeal

Claims on appeal are claims 1-18.

IV. Status of Amendments

There are no outstanding un-entered amendments before the Examiner. There are no un-entered amendments After Final.

V. Summary of Claimed Subject Matter

The present invention relates generally to configurable input/output buses for computers.

Claim 1

Independent claim 1 recites a configurable I/O bus architecture, comprising:

a system bus interface device (See Instant specification in at least page 2, Lines 16-17, page 3, Lines 11-22, and Figure 1, element 104);

first and second I/O bus interface devices (See Instant specification in at least page 2, Lines 17-21, page 3, Lines 23-26, and Figure 1, elements 106, 108);

first and second intermediate buses (See Instant specification in at least page 2, Lines 18-21, page 4, Lines 1-9, and Figure 1, elements 118, 120);

a switching device (See Instant specification in at least page 2, Lines 18-21, page 4, Lines 1-9, and Figure 1, element 114); and

a steering signal (See Instant specification in at least page 2, Lines 20-21, page 4, Lines 1-9, page 4, Line 10 through page 5, Line 7, and Figure 1, element 116); wherein:

the first intermediate bus couples the system bus interface device to the first I/O bus interface device (See Instant specification in at least page 2, Lines 17-18, page 4, Lines 1-3, and Figure 1, element 118);

the second intermediate bus directly couples the system bus interface device to the switching device (See Instant specification in at least page 2, Lines 18-20, page 4, Lines 2-3, and Figure 1, element 120); and

the switching device is operable to couple the second intermediate bus either to the first or to the second I/O bus interface device responsive to the steering signal (See Instant specification in at least page 2, Lines 18-21, page 4, Lines 3-5, page 4, Lines 5-9, page 4, Line 10 through page 5, Line 7, and Figure 1, element 114).

Claim 11

Independent claim 11 recites a configurable I/O bus architecture, comprising:

a system bus interface device (See Instant specification in at least page 2, Lines 16-17, page 3, Lines 11-22, and Figure 1, element 104);

first and second I/O bus interface devices (See Instant specification in at least page 2, Lines 17-21, page 3, Lines 23-26, and Figure 1, elements 106, 108);

a switching device arranged to be responsive to a steering signal (See Instant specification in at least page 2, Lines 18-21, page 4, Lines 1-9, and Figure 1, element 114);

a first intermediate bus coupling I/O bandwidth of the first I/O bus interface device with I/O bandwidth of the system bus interface device (See Instant specification in at least page 2, Lines 17-18, page 4, Lines 1-3, and Figure 1, element 118); and

a second intermediate bus coupling I/O bandwidth of the switching device with I/O bandwidth of the system bus interface device (See Instant specification in at least page 2, Lines 18-20, page 4, Lines 2-3, and Figure 1, element 120); wherein:

the switching device is arranged to couple I/O bandwidth of the second intermediate bus to I/O bandwidth of either the first or second I/O bus interface device responsive to the steering signal (See Instant specification in at least page 2, Lines 18-

21, page 4, Lines 3-5, page 4, Lines 5-9, page 4, Line 10 through page 5, Line 7, and Figure 1, element 114).

Claim 16

Independent claim 16 recites an I/O bus architecture comprising:

at least one first I/O bus interface device (See Instant specification in at least page 2, Lines 17-21, page 3, Lines 23-26, and Figure 1, element 106);

at least one second I/O bus interface device (See Instant specification in at least page 2, Lines 17-21, page 3, Lines 23-26, and Figure 1, element 108);

a switching device connected to the at least one first I/O bus interface device and the at least one second I/O bus interface device (See Instant specification in at least page 2, Lines 18-21, page 4, Lines 1-9, and Figure 1, element 114); and

a system bus interface device connected to the at least one first I/O bus interface device and the switching device (See Instant specification in at least page 2, Lines 16-17, page 3, Lines 11-22, and Figure 1, element 104);

wherein the switching device is arranged to connect the system bus interface device to one of the at least one first I/O bus interface device and the at least one second I/O bus interface device responsive to a steering signal (See Instant specification in at least page 2, Lines 18-21, page 4, Lines 3-5, page 4, Lines 5-9, page 4, Line 10 through page 5, Line 7, and Figure 1, element 114).

VI. Grounds of Rejection to be Reviewed on Appeal

A. The issue is whether claims 1-4, 9-14, and 16-18 are unpatentable under 35 U.S.C 103(a) as being obvious over *Lin* (US Published Patent Application 2003/0046499) in view of *Ajanovic* (US 5,859,988).

B. The issue is whether claims 5-8 and 15 are unpatentable under 35 U.S.C 103(a) as being obvious over *Ajanovic* in view of *Alexander* (US 6,510,529).

VII. Argument

A. Was the PTO correct in rejecting claims 1-4, 9-14, and 16-18 under 35 U.S.C. 103(a) as being obvious over *Lin* in view of *Ajanovic*?

Claim 1

The rejection of claims 1-4, 9-14, and 16-18 as being unpatentable over *Lin* in view of *Ajanovic* is hereby traversed.

1. The PTO has failed to specifically identify which elements of *Lin* correspond to the claimed subject matter

First, the PTO has failed to identify with any degree of precision which element of *Lin* is believed to correspond to the claimed system bus interface device. The PTO states "Figure 4 illustrates a computer system comprising mass storage devices coupled directly and indirectly to the CPU interface." Final Official Action (FOA) mailed December 26, 2007 at page 2, section 4. The PTO fails to specify whether the computer system, mass storage devices, or an unidentified, vague reference to "the CPU interface" is believed to correspond to the claim feature.

There appear to be several references to a computer system in *Lin*, none of which appear to be referring to the computer system as a system bus interface device. Additionally, Figure 4 is described as illustrating an "exemplary data processing system." Had the PTO meant to refer to the data processing system, Appellants believe the term data processing system or the term and corresponding reference numeral would have been used for clarity, i.e., "host 400." Thus, Appellants do not believe that the PTO is referring to host 400 of Figure 4.

As recited by the PTO, there appear to be several mass storage devices in Figure 4, i.e., mass storage 204A, 204B, 204C, and not one of them has been specifically identified by the PTO as corresponding to the claimed system bus interface device. Without an identification of a particular mass storage device under consideration, Appellants are unable to discern and succinctly address the various permutations of interpretations raised by the PTO. Because the PTO has not identified a particular mass storage device, Appellants do not believe that the PTO is referring to any of the mass storage devices as corresponding to the claimed system bus interface device.

Despite the PTO apparent reliance on "CPU interface," there appear to be no references to CPU interface in *Lin*. Instead, *Lin* recites a bus interface 402 which is connected with a bus (also labeled 402) which is referred to as either a host bus, a system bus, or a local bus in different portions of *Lin*. Based on at least the foregoing, Appellants believe that the PTO may be attempting to rely upon bus interface 402 as corresponding to the claimed system bus interface device; however, the PTO has failed to set forth with specificity whether Appellants understanding is correct. For at least this reason, reversal of the rejection is respectfully requested.

Appellants already requested clarification from the PTO regarding which elements of the reference are believed to correspond to the claim limitations. See Appellants' submission of June 11, 2007. Appellants renew the request for specificity by the PTO.

2. The PTO incorrectly recites a direct connection between mass storage 204B and CPU 401

Second, the PTO asserts that *Lin* discloses "a CPU 401 coupled directly to a mass storage device via first bus, local bus" without specifically identifying the mass storage device relied on, i.e., either mass storage device 204A, 204B, or 204C. See FOA at page 2, section 4. However, the PTO appears to specify that the intended mass storage device is device 204B with reference to the first intermediate bus coupling the system bus interface device. See FOA at page 3, Lines 1-3. This is incorrect because (contrary to the PTO's preceding statement) mass storage device 204B appears to be coupled with bus interface 402 indirectly via external memory interface 403 (Figure 4) and not directly as asserted. For at least this reason, reversal of the rejection is respectfully requested.

3. *Lin* fails to disclose a second intermediate bus directly coupling a system bus interface device to the switching device

Third, the PTO asserts that *Lin* discloses a "PCI bus - second bus coupling device 204C" to the switching device. This is incorrect because PCI bus 405 of *Lin* fails to directly couple bus interface 402 (based on the foregoing understanding of system bus interface device as set forth by the PTO) with bus control/bridge 407. Instead, PCI bus 405 directly couples bus control/bridge 407 with mass storage 204C. For at least this reason, reversal of the rejection is respectfully requested.

4. *Lin* fails to disclose a switching device operable to couple the second intermediate bus to the second I/O bus interface device responsive to the steering signal

Fourth, *Lin* fails to disclose a "switching device . . . operable to couple the second intermediate bus either to the first or to the second I/O bus interface device responsive to the steering signal" as claimed in claim 1. The PTO asserts that bus control 407 provides the claimed capability, however, this is incorrect.

Bus control 407 fails to couple the second intermediate bus (believed to be asserted as PCI bus 405 by the PTO, see FOA at page 2, section 4, Lines 8-10) to the second I/O bus interface device (believed to be asserted as mass storage device 204C, see FOA at page 2, section 4, Lines 5-7. Specifically, the *Lin* PCI bus 405 appears to be coupled to mass storage device 204C regardless of bus control 407 operation. PCI bus 405 of *Lin* appears to be coupled to mass storage device 204C without dependence on bus control 407. For at least this reason, reversal of the rejection is respectfully requested.

Further, as admitted by the PTO, bus control 407 fails to couple the second intermediate bus responsive to the steering signal.

5. *Ajanovic* fails to disclose a steering signal as claimed

Fifth, *Ajanovic* fails to disclose a steering signal to which the switching device is responsive, nor does *Ajanovic* appear to disclose a switching device operable to couple the second intermediate bus either to the first or to the second I/O bus interface device responsive to the steering signal as claimed in claim 1.

The PTO asserts that *Ajanovic* describes a steering signal to which a switching device is responsive. This is incorrect. The PTO-identified portion of *Ajanovic*, reproduced herein for ease of reference, states:

> Similarly, port C, comprising master/target interface 303, is coupled to the other secondary PCI bus 207. Port A 301 is coupled to port A/B data buffers 304 which is in turn coupled to port B 302. Port B 302 is coupled to port B/C data buffers 305 which is in turn coupled to port C 303. Port C 303 is coupled to port A/C data buffers 306 which is in turn coupled to port A 301. In addition, port A 301, port B 302, and port C 303 are each coupled to port B/C arbitration and control unit 308.
>
> *Ajanovic* at column 5, Line 65-column 6, Line 3.

The above portion of *Ajanovic* fails to describe a steering signal nor a steering signal to which a switching device is responsive. The above portion of *Ajanovic* appears to describe the coupling of ports A, B, and C to port B/C arbitration and control unit 308 without describing a steering signal or a switching device operable responsive to the steering signal. For at least this reason, reversal of the rejection is respectfully requested.

The PTO also attempts to rely on the following portion of *Ajanovic*, reproduced herein for ease of reference, which states:

> When the target bus is available, the triple-port bridge begins a read transaction on the target bus. The bridge continues to indicate a retry to the bus master on the initiating bus until the bridge has obtained the

> requested data from the target. In addition to the requested data, the triple-port bridge stores additional data from nearby addresses into the appropriate read pre-fetch buffer between the initiating bus interface and the target bus interface within the bridge. Once this data has been loaded into the read pre-fetch buffer, the triple-port bridge then accepts the read transaction that matches the original address and presents the buffered data. If the bus master on the initiating bus requests the additional data stored within the bridge's read pre-fetch buffer, the bus master continues to read the additional data. Any unread data remaining within the read pre-fetch buffer is discarded. Note that this read transaction applies to triple-port bridge operation regardless of which of the three buses coupled to the triple-port bridge is the initiating bus, and which of the remaining two buses is the target bus.
>
> For an alternate embodiment of the present invention, when a bus master on an initiating bus initiates a read transaction to a target on a target bus, the triple-port bridge does not save the address and command off the initiating bus. Instead, the triple-port bridge first determines if the target bus is busy. If the target is busy, the bridge indicates that the bus master should retry at a later time. If the target bus is not busy, the triple-port bridge forwards the request to the target bus to retrieve the data from the target, and forwards the data back to the initiating bus for the master.
>
> *Ajanovic* at column 8, Lines 5-34.

The above portion of *Ajanovic* fails to describe a steering signal or a steering signal to which a switching device is responsive.

The relied-on portion of *Ajanovic* fails to disclose that arbitration and control unit 308 is operable to couple the second intermediate bus either to the first or to the second I/O bus interface device. That is, the arbitration and control unit 308 appears to be coupled to both port B master/target (M/T) interface 302 and port C M/T interface 303 without dependency on receipt of a signal. For at least this reason, reversal of the rejection is respectfully requested.

6. No prima facie case of obviousness

Fourth, the PTO has failed to set forth a prima facie case of obviousness with respect to the combination of *Lin* with *Ajanovic*. Specifically, the PTO has failed to identify an articulated reasonable rationale or teaching, suggestion or motivation in either reference indicating why a person of ordinary skill would be motivated to combine the *Ajanovic* bridge in the drive controller of *Lin*. As previously set forth, *Lin* appears to already contemplate adding additional devices to a PCI system bus, see e.g., paragraph 49 of *Lin*. For at least this reason, reversal of the rejection is respectfully requested.

Further, the PTO reference to *Lin* at column 2, Lines 50-58 is not understood because *Lin* comprises only pages and paragraphs. Further still, column 2, Lines 50-58 (read as page 1, last portion of paragraph 11 through the first portion of paragraph 12) fails to identify the asserted motivation relied on by the PTO. Further still, column 2, Lines 50-58 of *Ajanovic* fails to describe the asserted motivation, as well. For at least this reason, reversal of the rejection is respectfully requested.

Based on each of the foregoing reasons, claim 1 is patentable over *Lin*, singly or in combination with *Ajanovic*, and the rejection is respectfully requested to be reversed.

Claims 2-4 and 9-10 depend, either directly or indirectly, from claim 1, include further limitations, and are patentable over *Lin* in view of *Ajanovic* for at least the reasons advanced above with respect to claim 1. The rejection of claims 2-4 and 9-10 should be reversed.

Claim 11 is patentable over *Lin*, singly or in combination with *Ajanovic*, for at least reasons similar to those advanced above with respect to claim 1 and the rejection should be reversed.

Further, claim 11 recites a coupling of I/O bandwidth between: first I/O bus interface device and the system bus interface device, switching device and the system bus interface device, and second intermediate bus and either of the first or second I/O bus interface devices which are not found in the applied combination of references. For at least this additional reason, reversal of the rejection is respectfully requested.

Claims 12-14 depend, either directly or indirectly, from claim 11, include further limitations, and are patentable over *Lin* in view of *Ajanovic* for at least the reasons advanced above with respect to claim 11. The rejection of claims 12-14 should be reversed.

Claim 16 is patentable over *Lin*, singly or in combination with *Ajanovic*, for at least reasons similar to those advanced above with respect to claim 1 and the rejection should be reversed.

Claims 17-18 depend, either directly or indirectly, from claim 11, include further limitations, and are patentable over *Lin* in view of *Ajanovic* for at least the reasons advanced above with respect to claim 11. The rejection of claims 17-18 should be reversed.

B. Was the PTO correct in rejecting claims 5-8, and 15 under 35 U.S.C. 103(a) as being obvious over *Ajanovic* in view of *Alexander*?

Claims 5-8 and 15

The rejection of claims 5-8 and 15 under 35 USC 103(a) as being unpatentable over *Ajanovic* in view of *Alexander et al.* (US Patent 6,510,529) is believed overcome in view of the foregoing arguments with respect to claims 1 and 11. Claims 5-8 and 15 depend, either directly or indirectly, from claims 1 and 11, include further features, and are patentable over *Ajanovic* in view of *Alexander* for at least the reasons advanced above with respect to claims 1 and 11. Reversal of the rejection is respectfully requested.

Further, the rejection of claims 5-8 and 15 is not understood in view of the fact that the PTO has failed to address the features of claims 1 and 11, from which the claims depend inter alia, with respect to *Ajanovic* or *Alexander*. That is, the PTO has not shown how either of *Ajanovic* or *Alexander* render obvious the features of claims 1 and 11 from which the claims depend. The PTO asserts a rejection of claims 1 and 11 in view of *Ajanovic* in combination with *Lin*; however, *Lin* has not been applied in the rejection of claims 5-8 and 15. For at least this reason, reversal of the rejection is respectfully requested.

VIII. Conclusion

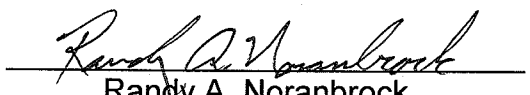
Each of the PTO's rejections has been traversed. Appellant respectfully submits that all claims on appeal are considered patentable over the applied art of record. Accordingly, reversal of the PTO's Final Rejection is believed appropriate and courteously solicited.

If for any reason this Appeal Brief is found to be incomplete, or if at any time it appears that a telephone conference with counsel would help advance prosecution, please telephone the undersigned, Appellant's attorney of record.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 08-2025 and please credit any excess fees to such deposit account.

Reversal of the rejection is in order.

Respectfully submitted,
Charles Hartman et al.

By: 

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IX. Claims Appendix

1. A configurable I/O bus architecture, comprising:

a system bus interface device;

first and second I/O bus interface devices;

first and second intermediate buses;

a switching device; and

a steering signal; wherein:

the first intermediate bus couples the system bus interface device to the first I/O bus interface device;

the second intermediate bus directly couples the system bus interface device to the switching device; and

the switching device is operable to couple the second intermediate bus either to the first or to the second I/O bus interface device responsive to the steering signal.

2. The configurable I/O bus architecture of claim 1:

further comprising at least a first signal indicating whether an I/O device is coupled to the second I/O bus interface device; and

wherein the steering signal is derived from the first signal such that the steering signal assumes a first state when the I/O device is so coupled and a second state when the I/O device is not so coupled.

3. The configurable I/O bus architecture of claim 2, wherein:

the switching device couples the second intermediate bus to the second I/O bus interface device when the steering signal assumes the first state, and couples the second intermediate bus to the first I/O bus interface device when the steering signal assumes the second state.

4. The configurable I/O bus architecture of claim 2:

further comprising a second signal indicating whether the I/O device is coupled to the second I/O bus interface device; and

wherein the steering signal is derived from both the first and second signals using a logic gate.

5. The configurable I/O bus architecture of claim 1:

further comprising a hand-operated switch; and

wherein the steering signal is derived from the hand-operated switch such that the steering signal assumes a first state when the hand-operated switch is in a first position, and assumes a second state when the hand-operated switch is in a second position.

6. The configurable I/O bus architecture of claim 5, wherein:

the switching device couples the second intermediate bus to the second I/O bus interface device when the steering signal assumes the first state, and

couples the second intermediate bus to the first I/O bus interface device when the steering signal assumes the second state.

7. The configurable I/O bus architecture of claim 2:

further comprising a hand-operated switch configured such that, when the hand-operated switch is in a first position, the state of the steering signal is unaffected, but when the switch is in a second position, the steering signal is forced into either its first or its second state.

8. The configurable I/O bus architecture of claim 4:

further comprising a hand-operated switch coupled to the output of the gate and configured such that, when the hand-operated switch is in a first position, the state of the steering signal is unaffected, but when the switch is in a second position, the steering signal is forced into either its first or its second state.

9. The configurable I/O bus architecture of claim 1:

wherein the first and second intermediate buses are rope buses.

10. The configurable I/O bus architecture of claim 1, wherein:

the switching device is operable to directly couple the second intermediate bus either to the first or to the second I/O bus interface device responsive to the steering signal.

11. A configurable I/O bus architecture, comprising:

a system bus interface device;

first and second I/O bus interface devices;

a switching device arranged to be responsive to a steering signal;

a first intermediate bus coupling I/O bandwidth of the first I/O bus interface device with I/O bandwidth of the system bus interface device; and

a second intermediate bus coupling I/O bandwidth of the switching device with I/O bandwidth of the system bus interface device; wherein:

the switching device is arranged to couple I/O bandwidth of the second intermediate bus to I/O bandwidth of either the first or second I/O bus interface device responsive to the steering signal.

12. The configurable I/O bus architecture of claim 11:

further comprising a first signal indicating whether an I/O device is coupled to the second I/O bus interface device; and

wherein the steering signal, in response to at least the first signal, indicates the I/O device coupled to the second I/O bus interface device and the I/O device not coupled to the second I/O bus interface device.

13. The configurable I/O bus architecture of claim 12, wherein:

the switching device couples the I/O bandwidth of the second intermediate bus to I/O bandwidth of the second I/O bus interface device in response to

the steering signal indicating the I/O device coupled to the second I/O bus interface device and couples the I/O bandwidth of the second intermediate bus to I/O bandwidth of the first I/O bus interface device in response to the steering signal indicating the I/O device coupled to the first I/O bus interface device.

14. The configurable I/O bus architecture of claim 12:

further comprising a second signal indicating whether an I/O device is coupled to the second I/O bus interface device; and

wherein the steering signal, in response to at least the first signal and the second signal, indicates the I/O device coupled to the second I/O bus interface device and the I/O device not coupled to the second I/O bus interface device.

15. The configurable I/O bus architecture of claim 11:

further comprising a hand-operated switch arranged to generate the steering signal, wherein the hand-operated switch in a first position generates the steering signal in a first state and the hand-operated switch in a second position generates the steering signal in a second state.

16. An I/O bus architecture comprising:

at least one first I/O bus interface device;

at least one second I/O bus interface device;

a switching device connected to the at least one first I/O bus interface device and the at least one second I/O bus interface device; and

a system bus interface device connected to the at least one first I/O bus interface device and the switching device;

wherein the switching device is arranged to connect the system bus interface device to one of the at least one first I/O bus interface device and the at least one second I/O bus interface device responsive to a steering signal.

17. The I/O bus architecture of claim 16, wherein:

further comprising a first signal indicating whether an I/O device is coupled to the at least one second I/O bus interface device; and

wherein the steering signal, in response to at least the first signal, indicates the I/O device coupled to the at least one second I/O bus interface device and the I/O device not coupled to the at least one second I/O bus interface device.

18. The I/O bus architecture of claim 17, wherein:

the switching device connects the at least one second I/O bus interface device to the system bus interface device in response to the steering signal

indicating the I/O device coupled to the second I/O bus interface device and couples the at least one first I/O bus interface device to the system bus interface device in response to the steering signal indicating the I/O device coupled to the first I/O bus interface device.

X. Evidence Appendix

None.

XI. Related Proceedings Appendix

None.